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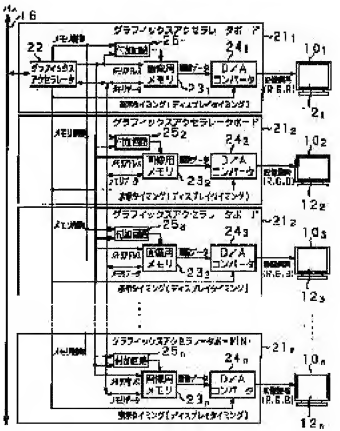
(54) CONTROL SIGNAL CONVERTER, METHOD, AND IMAGE PROCESSING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To achieve cost and space-saving by making do with a single graphics accelerator which is a plotting processing means, when configuring a multi- screen graphics system for controlling plural screens.

SOLUTION: Video signals from plural (n-pieces) graphics accelerator boards 211, 212, 213, 21n are being sent to n-pieces of display devices 101, 102, 103,..., 10n for a multi-screen display, respectively. Image data from one graphics accelerator 22 is sent to each of the image memories (video RAM) 231, 232, 233,..., 23n of the graphics accelerator boards 211, 212, 213,..., 21n, and also a control signal for accessing to the memories is sent to each additional circuit 251, 252, 253..., 25n, and a memory control signal is sent only to the memory for the image specified by the graphics accelerator 22.



* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention about a control signal inverter, a method, and an image processing device, It is related with the control signal inverter which changes the control signal from the drawing device of the multiscreen graphics system which arranges two or more display screens and constitutes a big screen especially to each display, a method, and the image processing device with which this control signal conversion art was applied.
[0002]
[Description of the Prior Art]A multiscreen graphics system which arranges each display screen of two or more displays in all directions, and constitutes a big screen is known conventionally.
[0003]Drawing 22 and drawing 23 show an example of the conventional outline composition of such a multiscreen graphics system.
[0004]In drawing 22, to display 10_1, two or more sets, for example, n stand, for constituting a multiscreen, 10_2, 10_3, ..., and 10_n. The video signal from graphics accelerator board (or card) 71_1 of n stand, 71_2, 71_3, ..., 71_n is sent, respectively.
[0005]To display 10_1 of n stand which was mentioned above for constituting a multiscreen in drawing 23, 10_2, 10_3, ..., and 10_n. The video signal from n graphics accelerator block 76_1, 76_2, 76_3, ..., 76_n is sent, respectively. Graphics accelerator block 76_1, 76_2, 76_3, ..., 76_n are used as the option substrate attached to the base board 70 for a multiscreen display, or a circuit block.
[0006]These graphics accelerator board 71_1, 71_2, 71_3, ..., 71_n or graphics accelerator block 76_1, 76_2, 76_3, ..., 76_n, All have the same composition and one arbitrary set of the graphics accelerator board 71 and the graphics accelerator blocks 76 has the graphics accelerator 72, the memory 73 for pictures (for example, Video RAM), and D/A converter 74.
[0007]It is shown that subscript k added to the reference number in a figure is a thing relevant to graphics accelerator board 71_k of eye k stand or graphics accelerator block 76_k.
For example, graphics accelerator board 71_1 has graphics accelerator 72_1, memory 73_1 for pictures,

and D/A converter 74 $_1$.

It is shown that the reference numbers without the subscript under explanation are one set of the arbitrary graphics accelerator board 71 and a thing relevant to the graphics accelerator block 76.

[0008]In such a graphics accelerator board 71 or the graphics accelerator block 76, the graphics accelerator 72 performs various drawing to the memory 73 for pictures (Video RAM), control of D/A converter 74, etc. The address signal of the memory 73 for pictures, a data signal, and a control signal are controlled. The memory 73 for pictures will accumulate image data, and the data will be rewritten by the graphics accelerator. The Video RAM (Video RAM) used as the memory 73 for pictures has two access ports (mouth of access), and one is a port for the graphics accelerator 72 to access.

Another is a port for performing a digital data output to D/A converter 74.

D/A converter 74 incorporates the image data in the memory 73 for pictures, and changes the digital data into the video signal of an analog, for example, red, and a green and blue video signal, and it has a role which generates a horizontal and vertical synchronizing signal. By this D/A converter 74, conversion and the generated signal are sent to the displays 10, such as a display, and is displayed as an image.

[0009]By providing display 10 $_1$ of n stand, 10 $_2$, 10 $_3$, ..., 10 $_n$, using this display 10 two or more sets, as shown in drawing 22 or drawing 23, and arranging in all directions, The multiscreen graphics system which realizes big screen high resolution is constituted. As the bus 16 in drawing 22 and drawing 23, For example, PCI (Peripheral Component Interconnect) Bus, An AGP (Accelerated Graphics Port) bus, Wide use of an ISA (e) bus, an EISA (ExtendedISA) bus, VL-Bus (VESA Local Bus), a VME bus, etc. and a standard bus, the bus that is completely exclusive use, etc. can be considered.

[0010]

[Problem(s) to be Solved by the Invention]Thus, in the former, when realizing a multiscreen graphics system, as composition for sending a video signal to two or more displays, Two or more graphics accelerator blocks 76 with the graphics accelerator 72, the memory 73 for pictures (Video RAM), and D/A converter 74 or graphics accelerator boards 71 had to be equipped.

[0011]Therefore, since the block which takes charge of one screen (screen), or multiscreen-ization in a board unit is needed, there is a fault that the cost of a graphics system will soar and the space of a graphics portion will also become big.

[0012]This invention is made in view of such the actual condition, and can be managed with addition of a necessary minimum component (parts), The circuit where performance is high is not needed but it aims at offer of a control signal inverter whose ****** provided with ** cost and the multiscreen control facility which realized space-saving becomes possible, a method, and an image processing device.

[0013]

[Means for Solving the Problem]In order that this invention may solve a technical problem mentioned above, a control signal inverter concerning this invention, A control signal inverter sent to two or more image memories which change a control signal from the above-mentioned drawing processing means in a multiscreen display system which sends image data from a drawing processing means to two or more displaying means, and on which it is displayed, and correspond to two or more above-mentioned displaying means is characterized by comprising:

A decode means which decodes an address which specifies two or more above-mentioned image

memories.
A selecting means which sends a memory control signal from the above-mentioned drawing processing means to an image memory to which it corresponds of two or more above-mentioned image memories according to an output from this decode means.

[0014]This invention a control signal converting method concerning this invention, In order to solve a technical problem mentioned above, A control signal converting method sent to two or more image memories which change a control signal from the above-mentioned drawing processing means in a multiscreen display system which sends image data from a drawing processing means to two or more displaying means, and on which it is displayed, and correspond to two or more above-mentioned displaying means is characterized by comprising:
A decoding process of decoding an address which specifies two or more above-mentioned image memories.
A process of sending a memory control signal from the above-mentioned drawing processing means to an image memory to which it corresponds of two or more above-mentioned image memories according to this decode output.

[0015]This invention is characterized by an image processing device comprising the following, in order to solve a technical problem mentioned above.
A drawing processing means which outputs image data for a multiscreen display.
Two or more image memories in which image data from this drawing processing means is accumulated.
Two or more displaying means which display each image data from two or more of these image memories, respectively.
A control signal conversion means which decodes an address which specifies two or more above-mentioned image memories, and sends a memory control signal from the above-mentioned drawing processing means to an image memory to which it corresponds of two or more above-mentioned image memories according to this decode output.

[0016]In such composition, a multiscreen display is attained with one control signal inverter.
[0017]
[Embodiment of the Invention]The desirable embodiment of the control signal inverter concerning this invention and a method is described referring to drawings.
[0018]The block diagram showing an example of the outline composition of the multiscreen graphic system with which the control signal inverter with which drawing 1 serves as an embodiment of the invention is applied, Drawing 2 is a block diagram showing other examples of the outline composition of the multiscreen graphic system with which the control signal inverter used as an embodiment of the invention is applied.
[0019]Two or more [first, / for constituting a multiscreen in drawing 1]. To for example, display 10_1 of n stand, 10_2, 10_3, ..., 10_n. The video signal from graphics accelerator board (or card) 21_1 of n stand, 21_2, 21_3, ..., 21_n is sent, respectively.

[0020]To display 10_1 of n stand which was mentioned above for constituting a multiscreen in drawing

2, 10_2, 10_3, ..., 10_n. The video signal from n graphics accelerator block 26_1, 26_2, 26_3, ..., and 26_n is sent, respectively, and is displayed on each display screen 12_1 - 12_n. Display screen 12_1 of these n sides - 12_n are arranged in all directions, and constitute the big screen. Graphics accelerator block 26_1, 26_2, 26_3, ..., 26_n are used as the option substrate attached to the base board 20 for a multiscreen display, or a circuit block.

[0021]These graphics accelerator board 21_1, 21_2, 21_3, ..., 21_n or graphics accelerator block 26_1, 26_2, 26_3, ..., and 26_n, Graphics accelerator board 21_1 and graphics accelerator block 26_1 have the same composition mutually, Each of graphics accelerator board 21_2, 21_3, ..., 21_n and graphics accelerator block 26_2, 26_3, ..., 26_n has the same composition.

[0022]Graphics accelerator board 21_1 and graphics accelerator block 26_1 are provided with the following.

The graphics accelerator 22 from which all serve as a drawing processing means.
The memory 23 for pictures (for example, Video RAM).
D/A converter 24.
The additional circuit 25 which changes the control signal from the graphics accelerator 22, and is sent to the memory 23 for pictures.

[0023]It is characterized by graphics accelerator board 21_2, 21_3, ..., and providing 21_n and graphics accelerator block 26_2, 26_3, ..., 26_n with the following.

The additional circuit 25 which all change the control signal from the graphics accelerator 22 of the above-mentioned graphics accelerator board 21_1 and graphics accelerator block 26_1, and send to the memory 23 for pictures.
The memory 23 for pictures.
D/A converter 24.

[0024]Here, subscript k added to the reference number in a figure is provided with the following.
It is shown that it is a thing relevant to graphics accelerator board 21_k of eye k stand or graphics accelerator block 26_k, for example, graphics accelerator board 21_1 is memory 23_1 for pictures.
D/A converter 24_1.

Although the graphics accelerator 22 is formed only in graphics accelerator board 21_1 (or graphics accelerator block 26_1 of the example of drawing 2) in the example of drawing 1, It is common use and they are other graphics accelerator board 21_2, 21_3, ..., 21_n (or graphics accelerator block 26_2, 26_3, ..., 26_n). In order to provide in any, The subscript is not attached. In this specification, the subscript is not given to the reference number of the thing relevant to one set of the arbitrary graphics accelerator board 21, and the graphics accelerator block 26, either.

[0025]The graphics accelerator 22 of graphics accelerator board 21_1 or graphics accelerator block 26_1

performs various drawing to the memory 23 for pictures (for example, Video RAM), control of D/A converter 24, etc. The address signal of the memory 23 for pictures, a data signal, and a control signal are controlled. The memory 23 for pictures will accumulate image data, and the data will be rewritten by the graphics accelerator. The Video RAM (Video RAM) used as the memory 23 for pictures, It has two access ports (mouth of access), one is a port for the graphics accelerator 22 to access, and another is a port for performing a digital data output to D/A converter 24. D/A converter 24 incorporates the image data in the memory 23 for pictures, and changes the digital data into the video signal of an analog, for example, red, and a green and blue video signal, and it has a role which generates a horizontal and vertical synchronizing signal. By this D/A converter 24, conversion and the generated signal are sent to the displays 10, such as a display, and is displayed on the display screen 12 as an image.

[0026]By providing display 10_1 of n stand, 10_2, 10_3, ..., 10_n, using this display 10 two or more sets, as shown in drawing 1 or drawing 2, and arranging in all directions, The multiscreen graphics system which realizes big screen high resolution is constituted. As the bus 16 in drawing 1 and drawing 2, it is PCI (Peripheral Component Interconnect), for example. Bus, AGP (Accelerated Graphics Port) Bus, Wide use of an ISA (Industrial Standard Architecture) bus, an EISA (Extended ISA) bus, VL-Bus (VESA Local Bus), a VME bus, etc., a standard bus, a bus which is completely exclusive use, etc. are mentioned.

[0027]In the embodiment of the invention shown in these drawing 1 and drawing 2, About graphics accelerator board 21_2, 21_3, ..., 21_n and graphics accelerator block 26_2, 26_3, ..., 26_n. By managing the composition of only using the additional circuit 25 for necessary minimum component 23, i.e., memory for pictures, and D/A converter 24, without providing a respectively individual graphics accelerator like before, ** cost and the multiscreen graphics system which realized space-saving are constituted.

[0028]The additional circuit 25 in such an embodiment is inserted to the control signal of the memory 23 for pictures which the graphics accelerator 22 of graphics accelerator board 21_1 or graphics accelerator block 26_1 controls. That is, it is a circuit which changes the control signal over the memory for pictures (Video RAM) which decodes a part of address which the graphics accelerator 22 publishes to the memory 23 for pictures (decoding), and is similarly published from the graphics accelerator 22.

[0029]the mechanism (2) which this additional circuit 25 decodes some of following two mechanisms, i. e., (1) address, (decoding), and changes the control signal over each memory -- it is realized from the mechanism in which the access cycle which needs to be simultaneously published to all the memory is identified.

[0030]The additional circuit 25 provided with these mechanisms can consider the case where it is the external circuit which became independent thoroughly [the graphics accelerator 22], and the case where it is the internal circuit where the circuit was included in the graphics accelerator 22.

[0031]Here, the control signal over a Video RAM is a RAS*:row address strobe (Row Address Strobe) signal concretely.

CAS*: Column-address strobe (Column Address Strobe) signal

WE*: Write enable (Write Enable) signal

OE*: Output enable (Output Enable) signal

DSF: Special function enabling (Special Function Enable) signal

** -- a signal [like] is pointed out. Among these control signals, the signal with which the sign of the

asterisk (*) is added expresses becoming with the Low level that it is effective (active), and generally calls it a negative logic signal. The signal with which the sign of the asterisk (*) is not added expresses becoming with the High level that it is effective (active), and generally calls it a positive logic signal.

[0032]Next, the example which shows the relation between each screen (screen) of a multiscreen and the memory for pictures in a graphics system (Video RAM) is explained, referring to drawing 3 and drawing 4. Each display 10_1 - display screen 12_1 of the 9th page of 10_9 - 12_9 are put in order and arranged in all directions [3x3] using nine sets of display 10_1 -, and 10_9, and the big screen of high resolution consists of examples of these drawing 3 and drawing 4.

[0033]In drawing 3, the graphics accelerator 22 performs drawing control to each Video RAM (memory for pictures) 23_1 - 23_9. These Video RAM 23_1 - 23_9, Nine sets of display 10_1 which constitutes a multiscreen -, each display screen 12_1 of 10_9 - 12_9 (drawing 4) are supported, The contents drawn by Video RAM 23_1 - 23_9 are displayed on display 10_1 - screen 12_1 of 10_9 - 12_9. Video RAM 23_1 - 23_9 are arranged in the address space which continues for the graphics accelerator 22, and are easy to perform calculation for drawing.

[0034]Although the high resolution big screen comprises an example of drawing 3 and drawing 4 by arranging nine sets of display 10_1 -, each display screen 12_1 of 10_9 - the 9th page of 12_9 by every direction 3x3, The graphics accelerator 22 is taking into consideration arrangement of these display screen 12_1 - 12_9, and performs suitable drawing to Video RAM 23_1 - 23_9. And the above-mentioned additional circuit 25 (additional circuit 25_1 [at the time of being referred to as n= 9 of drawing 1 and drawing 2] - 25_9) as a translator of the control signal by an embodiment of the invention is formed between the graphics accelerator 22, and each Video RAM 23_1 - 23_9.

[0035]The additional circuit 25 which is this control signal translator in drawing 3, Top 4 bits of the address published in order that the graphics accelerator 22 may access Video RAM (memory for pictures) 23_1 - 23_9 are decoded (decoding), It judges access to which Video RAM of Video RAM 23_1 - 23_9 it is, and only the memory control signal over the meant Video RAM, for example, k-th Video RAM ($1<=k<=9$) 23_k, is validated.

[0036]Therefore, for the graphics accelerator 22, for example, the appropriate access cycle meant, it will be published to k-th Video RAM 23_k. In order to display the contents of Video RAM 23_k, D/A converter (drawing 1, 24_k of drawing 2) located in the preceding paragraph of display 10_k in the contents When the graphics accelerator 22 starts the lead transfer cycle for sending in, or a split lead transfer cycle, Detect the cycle and in 1 time of a lead transfer cycle, or a split transfer cycle. A memory control signal is changed so that it may become the lead transfer cycle or split lead transfer cycle to all the Video RAM 23_1 - 23_9.

[0037]A concrete example is given and explained in full detail about such an additional circuit 25. Explanation about the control signal conversion according to cycle is performed to the beginning. Next, whether the access cycle to Video RAM 23 is control signal conversion of as opposed to [it is single, for

example,] k-th Video RAM 23 $_k$. Although it must judge by a cycle whether it is control signal conversion to all Video RAM 23 $_1$ - 23 $_9$, explanation about the cycle discernment for performing the judgment is performed.

[0038]At the example of this embodiment, it is 1 pixel = 8 bits (namely, eight bits per pixel). Resolution: Assume the graphics system of conditions like 1024 pixels by 1024 pixels. The capacity of the Video RAM corresponding to one display in this case is 1024x1024x8 bit =8M bit =1 M byte (1MByte).

It becomes. If the start address of an image memory (Video RAM group 23 $_1$ - 23 $_9$) is set to 0x000000 (it is shown that 0x is a hexadecimal number display.), The relation between the start address of each Video RAM (respectively 1MByte), the image drawn there, and the whole high resolution big screen becomes like drawing 5.

[0039]The above-mentioned graphics accelerator 22 writes image 13 $_1$ to display on display screen 12 $_1$ of drawing 5 - 12 $_9$, respectively - 13 $_9$ in each Video RAM 23 $_1$ - 23 $_9$. For example, the above-mentioned graphics accelerator 22 performs drawing access, for example, rectangle drawing, straight-line drawing, etc., to Video RAM 23 $_1$, etc. to display a picture (picture) like image 13 $_1$ of drawing 5 on 1st display screen 12 $_1$. The access addresses at this time are 0x00_0000 - 0x0 f_ffff. Drawing access is performed to Video RAM 23 $_2$ and the access address at that time serves as 0x10_0000 - 0x1 f_ffff to display a picture (picture) like image 13 $_2$ of drawing 5 on 2nd display screen 12 $_2$. Like the following to display a picture (picture) like image 13 $_3$ of drawing 5 - 13 $_9$ on the 3rd - the 9th display screen 12 $_3$ - 12 $_9$. Perform drawing access to Video RAM 23 $_3$ - 23 $_9$, and the access address at that time, Respectively 0x20_0000 - 0 x2f_ffff, 0x30_0000 - 0x3 f_ffff, It becomes 0x40_0000 - 0x4 f_ffff, 0x50_0000 - 0x5 f_ffff, 0x60_0000 - 0x6 f_ffff, 0x70_0000 - 0x7 f_ffff, and 0x80_0000 - 0x8 f_ffff.

[0040]Namely, although the number of bits of an address required for each Video RAM 23 $_1$ - 23 $_9$ to access, respectively (a part for 1MByte) is 20 bits (A_0 - A_{19}), In order to specify one in nine Video RAM 23 $_1$ - 23 $_9$, a 4-bit address is needed, this is added to the higher rank side, and a 24 bits (A_0 - A_{23}) address is needed on the whole.

[0041]The conversion circuit 25 which is a control signal translator part by an embodiment of the invention to these accesses, only receiving k-th Video RAM 23 $_k$, for example, it decoded top 4 bits (A_{20} - A_{23}) of the access address (decoding) and the graphics accelerator 22 meant -- a memory control signal -- issue -- that is, it activates. It is made for the memory control signal to other Video RAMs to become with a stationary state (in i.e., the state [it is inactive]).

[0042]On the other hand, when the graphics accelerator 22 publishes a lead transfer cycle or a split lead transfer cycle, The conversion circuit 25 which is a control signal converter by an embodiment of the invention, a lead transfer cycle or a split lead transfer cycle is simultaneously started to all the Video RAM 23 $_1$ - 23 $_9$ -- as -- a memory control signal -- issue -- that is, it activates. Since the display which constitutes each screen of a multiscreen is a thing of an identical kind, The display timing (display

timing) sent out by the picture image data sent out by the D/A converter and the graphics accelerator, It is altogether the same to display 10_1 - 10_9, Therefore, the lead transfer cycle or split lead transfer cycle which a graphics accelerator must start in order to send out the image data which is the contents of the Video RAM to a D/A converter, It is possible to publish in parallel simultaneously to all the Video RAM 23_1 - 23_9, and it is more efficient. As a result, unlike the conventional method which is carrying out the control of the one Video RAM in its duty by one graphics accelerator, all the Video RAMs can be efficiently controlled now by forming the mechanism by an embodiment of the invention in a single graphics accelerator. Simultaneously, the effect that space-saving-ization of the system itself is attained is also acquired by the ability to reduce cost reduction and part mark by the ability to reduce the number of a graphics accelerator.

[0043]Next, the concrete example of control signal conversion is explained with drawing 6.

[0044]In the example of drawing 6, the graphics accelerator 22 has published a 24 bits (A_0 - A_{23}) address, for example, 0x11_2400, for example in the access cycle to 2nd Video RAM 23_2. When the graphics accelerator 22 starts except a lead transfer cycle or a split lead transfer cycle, here, The additional circuit 25 which is a control signal converter is top 4 bits (A_{20} - A_{23}) of this address. 0x1 (hexadecimal number) is decoded (decoding), The access cycle started by the graphics accelerator 22 judges that it is access to Video RAM 23_2. And the additional circuit 25 which is the converter which received top 4 bits (A_{20} - A_{23}) of an address, Only the memory control signal over Video RAM 23_2 is made effectively, i.e., active, and the memory control signal over other Video RAM 23_1 and Video RAM 23_3 - 23_9 is left an invalid state, i.e., an inactive state. When a graphics accelerator starts a lead transfer cycle or a split lead transfer cycle, When the access cycle identification part (an action is mentioned later) by an embodiment of the invention identifies the cycle, a control signal converter validates the memory control signal over all the Video RAM 23_1 - 23_9 (active).

[0045]Therefore, the lead transfer address to Video RAM 23_1 - 23_9, It is set to 0x01_2400, 0x11_2400, 0x21_2400, 0x31_2400, 0x41_2400, 0x51_2400, 0x61_2400, 0x71_2400, and 0x81_2400, respectively, The lead transfer of the same position (address) will be carried out relatively [each Video RAM]. the data of the same position of the screen expressed by Video RAM 23_1 of this, i.e., nine pieces, - 23_9 -- simultaneous -- every -- it will send out to a D/A converter.

[0046]Next, the example of the circuit for decoding top 4 bits (A_{20} - A_{23}) address for choosing any one of Video RAM 23_1 mentioned above - the 23_9 (decoding), It is shown in (a) - (e) of the following drawing 7, (f) of drawing 8 - (i), and drawing 9.

[0047]In (f) - (i) of (a) - (e) of drawing 7, and drawing 8, Top 4 bits (A_{20} - A_{23}) address of the 24 bits (A_0 - A_{23}) addresses for accessing the whole memory 23 for described images (Video RAM) is decoded (decoding), The circuit which generates selection signal S_k for choosing one Video RAM used as an accessing object, for example, k-th Video RAM 23_k, is shown.

[0048]For example, by top 4 bits (A_{20} - A_{23}) address signal being sent to an AND gate by each via an

inverter in the circuit of (a) of drawing 7, top 4 bits (A_{20} - A_{23}) the case of 0x0 (it is 0000 at a binary number) -- selection signal S_1 from an AND gate -- being effective, active : positive logic "1", i.e., a High level, -- it becomes and 1st Video RAM 23 $_1$ is chosen. In the circuit of (b) of drawing 7 like the following, Top 4 bits In the case of 0x1 (it is 0001 at a binary number), selection signal S_2 of 2nd Video RAM 23 $_2$ becomes effective, and by the circuit of (c) of drawing 7. Top 4 bits In the case of 0 x2 (it is 0010 at a binary number), selection signal S_3 of 3rd Video RAM 23 $_3$ becomes effective, and by the circuit of (d) of drawing 7. Top 4 bits In the case of 0x3 (it is 0011 at a binary number), selection signal S_4 of 4th Video RAM 23 $_4$ becomes effective, and by the circuit of (e) of drawing 7. Top 4 bits In the case of 0x4 (it is 0100 at a binary number), selection signal S_5 of 5th Video RAM 23 $_5$ becomes effective. They are the same, and in (f) of drawing 8. [of (f) of drawing 8 - (i)] Top 4 bits In the case of 0x5 (it is 0101 at a binary number), selection signal S_6 of 6th Video RAM 23 $_6$ becomes effective, and in (g) of drawing 8. Top 4 bits In the case of 0x6 (it is 0110 at a binary number), selection signal S_7 of 7th Video RAM 23 $_7$ becomes effective, and in (h) of drawing 8. Top 4 bits In the case of 0x7 (it is 0111 at a binary number), selection signal S_8 of 8th Video RAM 23 $_8$ becomes effective, and in (i) of drawing 8. In top 4 bits, in the case of 0x8 (it is 1000 at a binary number), selection signal S_9 of 9th Video RAM 23 $_9$ becomes effective.

[0049]The example of the whole decipherment (decoding) circuit which unified all the circuits shown by (a) - (e) of above-mentioned drawing 7 and (f) of drawing 8 - (i) is shown in following drawing 9.

[0050]Next, it explains, referring to the following drawing 10 and drawing 11 for the example of a circuit of changing a memory control signal.

[0051]In drawing 10, when cycles other than a lead transfer cycle or a split lead transfer cycle are started by the graphics accelerator, the inside of nine Video RAM 23 $_1$ generated by the decipherment (decoding) circuit 27 - selection signal S_1 of 23 $_9$ - S_9 -- one -- being effective (active = High level), [become and] Therefore, only the control signal (RAS*, CAS*, WE*, OE*) of the negative logic to the selected Video RAM is effective (active = Low level). It becomes. When a lead transfer cycle or a split lead transfer cycle is started by the graphics accelerator, It is not concerned with selection signal S_1 of the Video RAM generated by the decipherment (decoding) circuit 27 - S_9, All nine Video RAM 23 $_1$ - 23 $_9$ are chosen, therefore the control signal (RAS*, CAS*, WE*, OE*) of the negative logic to all the Video RAMs is effective (active = Low level). It becomes.

[0052]In [in order to realize such operation] drawing 10, A signal as shows that a lead transfer cycle and a split lead transfer cycle are starting, For example, signal RTC set to a High level during lead transfer cycle starting, Using the signal SRTC set to a High level while a split lead transfer cycle starts, or this signal RTC (or SRTC), each with the above-mentioned Video RAM 23 $_1$ - selection signal S_1 of 23 $_9$ - S_9 -- NOR (nondisjunction) being taken and with these NOR outputs. each with the control signal

(RAS*, CAS*, WE*, OE*) of the above-mentioned negative logic -- he is trying to obtain each Video RAM 23_1 - control signal CS_1 of 23_9 - CS_9 by taking OR (logical sum)

[0053]In drawing 11, a lead transfer cycle. Or when cycles other than a split lead transfer cycle are started by the graphics accelerator, the inside of nine Video RAM 23_1 generated by the decipherment (decoding) circuit 27 - selection signal S_1 of 23_9 - S_9 -- one -- being effective (active = High level), [become and] therefore, the control signal (DSF) of the positive logic to the selected Video RAM -- being effective (active = High level) -- it becomes. When a lead transfer cycle or a split lead transfer cycle is started by the graphics accelerator, it is not concerned with the selection signal of RAM generated by the decipherment (decoding) circuit, but all nine Video RAM 23_1 - 23_9 are chosen -- therefore, the control signal (DSF) of the positive logic to all the RAM -- being effective (active = High level) -- it becomes.

[0054]For this reason, signal RTC (or signal SRTC set to a High level while a split lead transfer cycle starts) set to a High level during lead transfer cycle starting in drawing 11, each with the above-mentioned Video RAM 23_1 - selection signal S_1 of 23_9 - S_9 -- OR (logical sum) being taken and with these OR outputs. each with the control signal (DSF) of the above-mentioned positive logic -- he is trying to obtain each Video RAM 23_1 - control signal CS_1 of 23_9 - CS_9 by taking AND (logical product)

[0055]The circuit shown in these drawing 10 and drawing 11 is provided in the additional circuit 25 which is a control signal conversion circuit in drawing 3 or drawing 6.

[0056]Next, the signal inputted into the control signal conversion circuit (equivalent to the additional circuit 25 of drawing 3 or drawing 6) which has a circuit as shown in drawing 10 and drawing 11 which were mentioned above, That is, explanation about the cycle discernment for making signal RTC set to a High level during the above-mentioned lead transfer cycle starting and the signal SRTC set to a High level during split lead transfer cycle starting is performed.

[0057]If the memory access cycle which a graphics accelerator publishes to the memory for pictures (Video RAM) is summarized first, as shown in following drawing 12 - drawing 19, eight kinds of access cycles exist.

[0058]Drawing 12 shows the read cycle containing a page mode, drawing 13 shows the write cycle containing a page mode, drawing 14 shows the block write cycle containing a page mode, and drawing 15 shows the lead modification write cycle containing a page mode. Drawing 16 shows a color-registers set cycle, and drawing 17 shows the CAS before RAS refresh cycle. Drawing 18 shows a lead transfer cycle and drawing 19 shows the split lead transfer cycle.

[0059]Each signal currently used in these drawing 12 - drawing 19 expresses the following meaning.

Address: Address signal
Data: Data signal
RAS*: Row address strobe (Row Address Strobe) signal
CAS*: Column-address strobe (Column Address Strobe) signal
WE*: Write enable (Write Enable) signal
OE*: Output enable (Output Enable) signal

DSF: Special function enabling (Special Function Enable) signal
Here, the signal with which the asterisk (*) sign is added expresses becoming with the Low level that it is effective (active), and generally says it as a negative logic signal. The signal which is not added expresses becoming with the High level that it is effective (active), and generally says it as a positive logic signal.
[0060]Two kinds of cycles, the above-mentioned lead transfer cycle and a split lead transfer cycle, are identified out of the access cycle shown in these drawing 12 - drawing 19. If the action of each control signal in each access cycle shown in these figures is taken into consideration, When a RAS* signal is a High level and OE* signal is set to a Low level as an example of the conditions for identifying a lead transfer cycle and a split lead transfer cycle, A lead transfer cycle and split lead transfer SAIKURURU begin, and the conditions of ending when a RAS* signal is set to a High level from a Low level are mentioned.
[0061]As an example, signal RTC of drawing 18 shows the signal set to a High level during lead transfer cycle starting, and the signal SRTC of drawing 19 shows the signal set to a High level during split lead transfer cycle starting.
[0062]Therefore, in the cycle identification scheme by an embodiment of the invention. Signal RTC which shows that a lead transfer cycle is starting taking advantage of the time of this condition being fulfilled, Or the signal SRTC which shows that a split lead transfer cycle is starting is used as a High level, Then, since it judges that the cycle is advancing and continues maintaining the signal at a High level until a RAS* signal is set to a High level (inactive) from a Low level (active), a Low level is used. Thereby, the signal is set to a High level while a lead transfer cycle or a split lead transfer cycle is starting.
[0063]The above-mentioned conditions are identified and the easy example of a circuit which generates the signal which shows that a lead transfer cycle or a split lead transfer cycle is starting is shown in the following drawing 20.
[0064]Only by d-type-flip-flop FF_1 and FF_2 which are represented with the example of drawing 20 by 7474 in what is called TTL74 series, etc., and a NAND gate. The signals RTC and SRTC which show that a lead transfer cycle or a split lead transfer cycle is starting are generated. Here the CLK (clock) signal inputted into d-type-flip-flop FF_1 and FF_2, It is a basic clock with which a graphics accelerator is also used, and the graphics accelerator has made each access cycle based on this clock. And the example of a circuit given here is an example to the last, and it is possible for the actions of the access cycle to differ delicately and to also consider the example of a circuit variously by the method of implementation (mounting) of each access cycle, according to it.
[0065]Next, the difference between a lead transfer cycle and a split lead transfer cycle is explained.
[0066]The block diagram which VRAM (Video RAM) simplified is shown in drawing 21. In this drawing 21, to VRAM (Video RAM). There are RAM port 31 and the serial port 32, and The above-mentioned read cycle, A write cycle, a block write cycle, a read-modified-write cycle, and a color-registers set cycle are cycles in which access is performed to the data in the memory cell array 33, or the various registers in a memory via RAM port 31. On the other hand, a lead transfer cycle and a split lead transfer cycle are cycles for sending out the data in the memory cell array 33 to the data register 35 via the transfer gate 34. And the difference between a lead transfer cycle and a split lead transfer cycle, As opposed to transmitting data to the data register 35 at once [all the / column] from the inside of the

memory cell array 33 in a lead transfer cycle, In a split lead transfer cycle, data is divided into the low rank side column and the higher rank side column from the inside of the memory cell array 33, and it transmits to the data register 35. The time of the time of a DSF signal (positive logic) continuing being a Low level being set to a High level at the time of falling of a lead transfer cycle and a RAS* signal (negative logic) of the difference on a cycle is a split lead transfer cycle.

[0067]According to the above embodiments of the invention, when realizing a multiscreen graphic system, it ends with addition of a necessary minimum component (parts), the graphics accelerator which is a drawing processor can be managed with one set, and the circuit (hardware) where performance is high is not needed. Therefore, construction of the high resolution big screen graphics system which it became possible to have ** cost and the multiscreen control facility which realized space-saving, namely, aimed at the show effect and the demonstration is attained.

[0068]This invention is not limited only to the embodiment mentioned above, and the number of screens which constitutes a multiscreen, or the number of a display is not limited to nine sets, but can constitute a multiscreen using the display of the arbitrary number which can be arranged in all directions, for example.

[0069]

[Effect of the Invention]According to this invention, so that clearly from the above explanation. In the case of the control signal conversion sent to two or more image memories which change the control signal from the above-mentioned drawing processing means in the multiscreen display system which sends the image data from a drawing processing means to two or more displaying means, and on which it is displayed, and correspond to two or more above-mentioned displaying means. By decoding the address which specifies two or more above-mentioned image memories, and sending the memory control signal from the above-mentioned drawing processing means to the image memory to which it corresponds of two or more above-mentioned image memories according to this decode output, The access control of two or more image memories can be carried out with necessary minimum composition by one set of a drawing processor, and it can contribute to the cost reduction of a multiscreen system, and space reduction.

[0070]The drawing processing means which outputs the image data for a multiscreen display according to the image processing device concerning this invention, Two or more image memories in which the image data from this drawing processing means is accumulated, Two or more displaying means which display each image data from two or more of these image memories, respectively, By decoding the address which specifies two or more above-mentioned image memories, and having a control signal conversion means which sends the memory control signal from the above-mentioned drawing processing means to the image memory to which it corresponds of two or more above-mentioned image memories according to this decode output, ** cost and the multiscreen system which realized space-saving can only consist of adding necessary minimum composition to one set of a drawing processor.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the outline composition of an example of the multiscreen graphics system with which the embodiment concerning this invention is applied.
[Drawing 2]It is a block diagram showing the outline composition of other examples of the multiscreen graphics system with which the embodiment concerning this invention is applied.
[Drawing 3]It is a figure for explaining the relation between the graphics accelerator of a multiscreen graphics system, and a Video RAM.
[Drawing 4]It is a figure showing the example of composition of the display screen of a multiscreen graphics system.
[Drawing 5]It is a figure showing the Video RAM of a multiscreen graphics system, the image drawn, and a relation with a display screen.
[Drawing 6]It is a figure for explaining the example of control signal conversion.
[Drawing 7]It is a figure showing the circuit for decoding the high order bit of the address for choosing two or more Video RAMs.
[Drawing 8]It is a figure showing the circuit for decoding the high order bit of the address for choosing two or more Video RAMs.
[Drawing 9]It is a figure showing an example of the whole decipherment (decoding) circuit which unified the circuit shown in drawing 7 and drawing 8.
[Drawing 10]It is a figure showing the example of a circuit of changing a memory control signal.
[Drawing 11]It is a figure showing the example of other circuits of changing a memory control signal.
[Drawing 12]It is a figure showing the read cycle containing a page mode.
[Drawing 13]It is a figure showing the write cycle containing a page mode.
[Drawing 14]It is a figure showing the block write cycle containing a page mode.
[Drawing 15]It is a figure showing the lead modification write cycle containing a page mode.
[Drawing 16]It is a figure showing a color-registers set cycle.
[Drawing 17]It is a figure showing a CAS before RAS refresh cycle.
[Drawing 18]It is a figure showing a lead transfer cycle.
[Drawing 19]It is a figure showing a split lead transfer cycle.

[Drawing 20]It is a figure showing an example of the circuit for generating the signal which shows that a lead transfer cycle and a split lead transfer cycle are starting.
[Drawing 21]It is a block diagram showing the outline composition of a Video RAM.
[Drawing 22]It is a block diagram showing the outline composition of an example of the conventional multiscreen graphics system.
[Drawing 23]It is a block diagram showing the outline composition of other examples of the conventional multiscreen graphics system.
[Description of Notations]
10 A display and 12 A display screen and 21 Graphics accelerator board, 22 A graphics accelerator and 23 The memory for pictures (Video RAM), 24 D/A converters, and 25 An additional circuit (control signal conversion circuit) and 26 Graphics accelerator block

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[Translation done.]

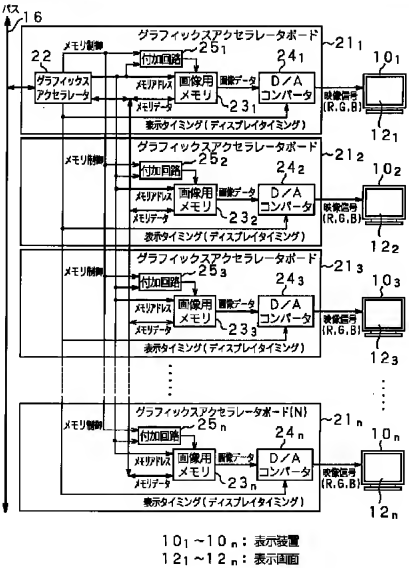
* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

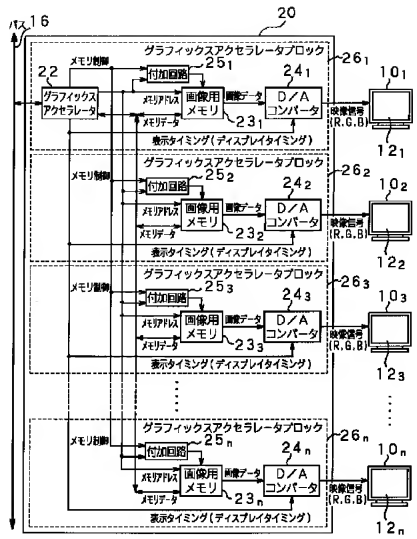
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

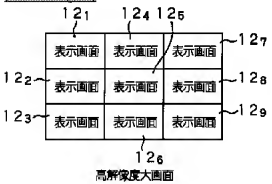
[Drawing 1]



[Drawing 2]



[Drawing 4]



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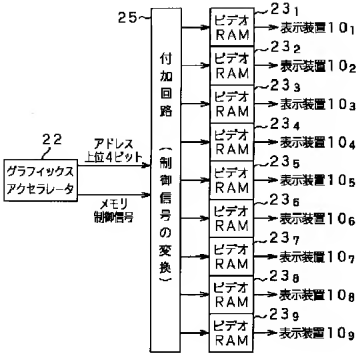
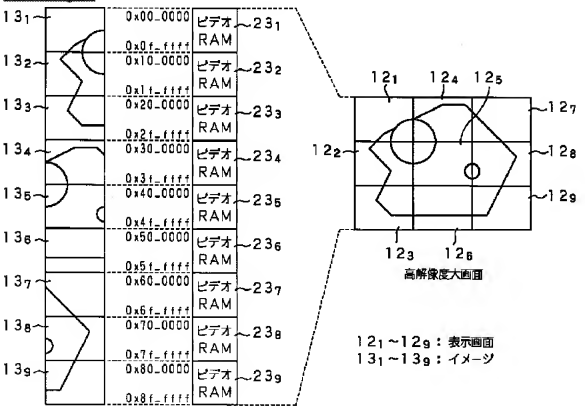
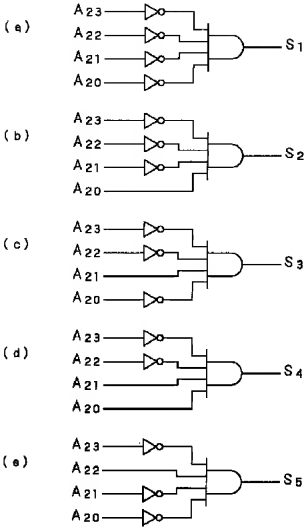


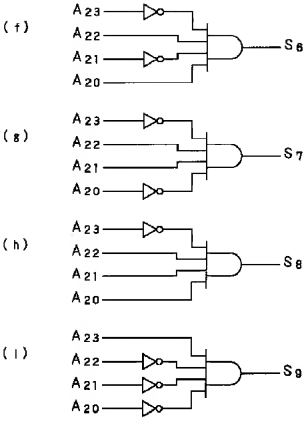
[Drawing 5]



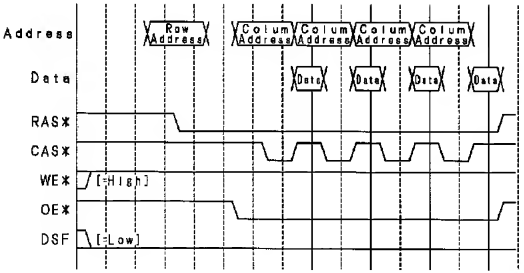
[Drawing 7]


(a)
A23
A22
A21
A20
S1
(b)
A23
A22
A21
A20
S2
(c)
A23
A22
A21
A20
S3
(d)
A23
A22
A21
A20
S4
(e)
A23
A22
A21
A20
S5

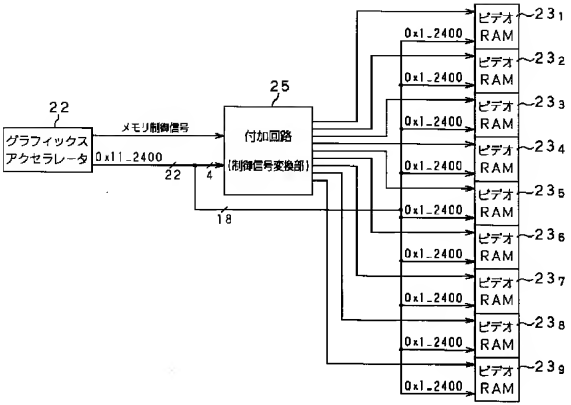
[Drawing 8]



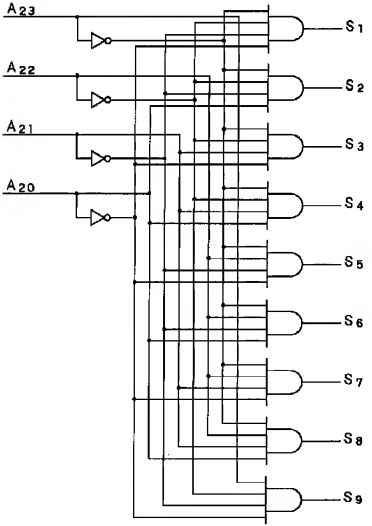
[Drawing 12]



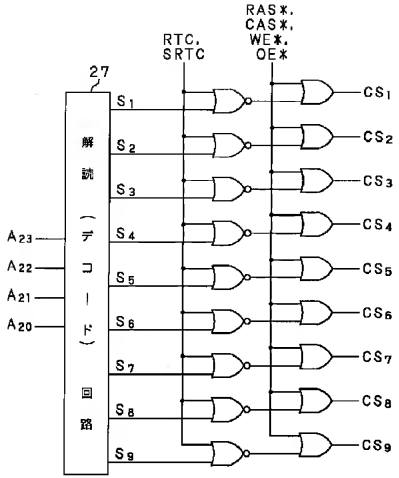
[Drawing 6]


22
グラフィックス
アクセラレータ
メモリ制御信号
0x11_2400
22
4
25
付加回路
(制御信号変換部)
18
0x1_2400
ビデオ
RAM
231
232
233
234
235
236
237
238
239

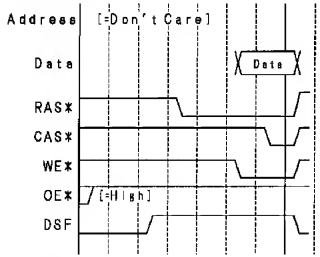
[Drawing 9]


A23
A22
A21
A20
S1
S2
S3
S4
S5
S6
S7
S8
S9

[Drawing 10]



[Drawing 16]



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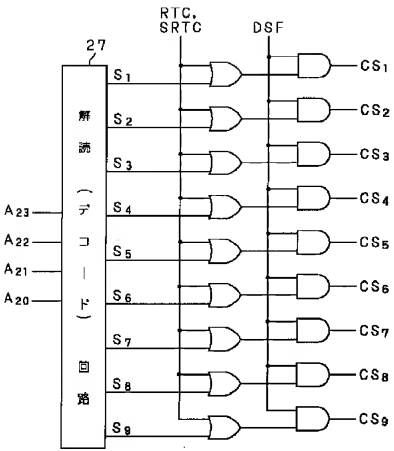
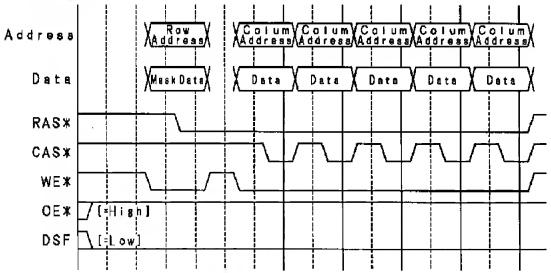
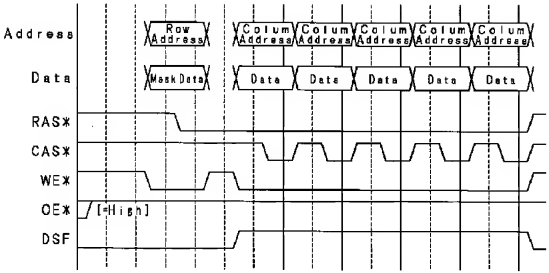


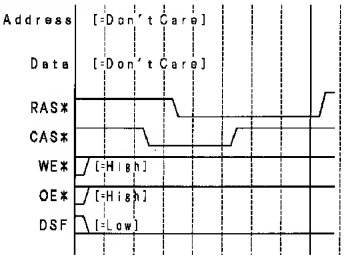
[Drawing 13]



[Drawing 14]



[Drawing 17]



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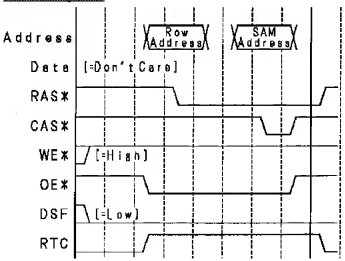

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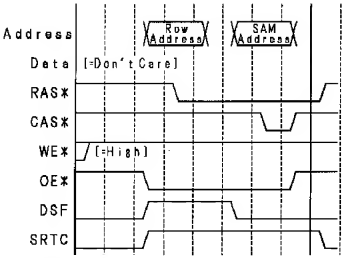

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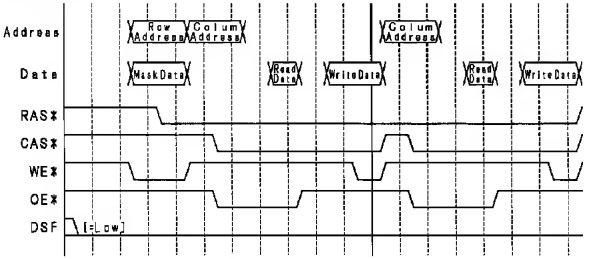
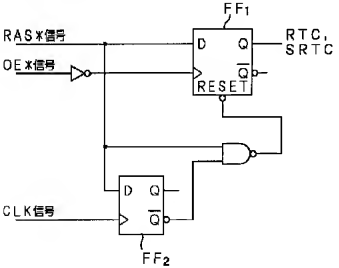


[Drawing 20]



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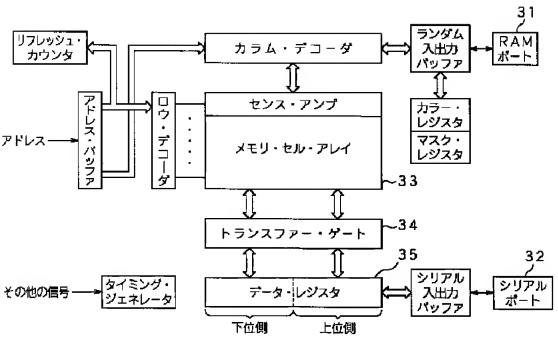

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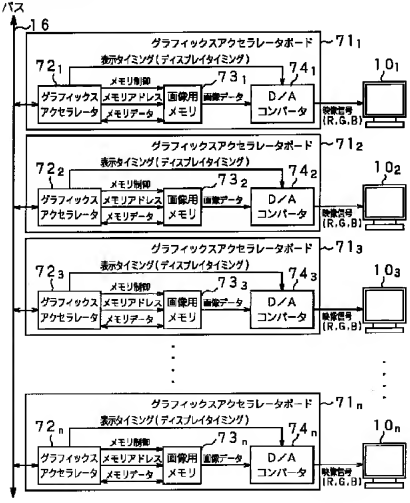
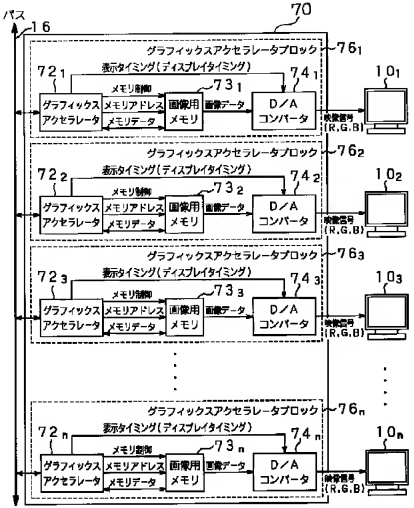


[Drawing 23]



[Translation done.]